KRISHANG TALSANIA

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Technical Skills

Languages: SystemVerilog/Verilog, C++, Python, Java, TCL, Bash Scripting, MATLAB, LaTeX

Technologies: FPGA Development, RISC-V, ROS2 / MoveIt2, RTOS, Fedora Linux, LLVM, GCC, AOSP

Tools & Concepts: Xilinx (Vivado & Vitis HLS), Synopsys Fusion Compiler, Hardware Abstraction Layers, Bare-metal Firmware

Experience

Project Intern — *May 2025 – July 2025*

Robotics Lab – IIT Gandhinagar

- Worked on an **18-DOF half-humanoid robot** under Prof. Harish PM (IITGN Robotics); developed MoveIt2 configs, URDF models, **Dynamixel drivers**, and an **actuator SDK** supporting extended position control, obstacle avoidance, and gesture recognition.
- Implemented **pick-and-place pipeline** with pre-grasp and pre-place waypoints; developed ROS2 actions, publishers, and listeners for full motion coordination.
- Achieved up to **2× faster IK convergence** by replacing KDL with a **Newton-Raphson solver** in Pinocchio as a custom MoveIt2 IK plugin.

Technical Content Intern — *March 2025 – May 2025*

My Equation (EdTech Startup)

- Authored technical documentation, case studies, and research articles on **Embedded Systems**, **Electric Vehicles**, and **ROS2**.
- Collaborated with technical mentors and industry experts to refine system-level documentation for educational resources.

Projects

Scalable 4-Core Mesh Network-on-Chip (NoC)

Packet-switched communication fabric – presented on Artix-7 100T (Nexys A7)

- Implemented parameterized **2×2 mesh NoC** in SystemVerilog; 5-port routers with deadlock-free **XY Dimension-Order Routing**, 5×5 round-robin switch allocator with packet-locking, and combinational AND-OR crossbar; **3.4 Gbps** per port at 100 MHz, **40.8 Gbps** peak fabric bandwidth.
- Integrated **UART protocol bridge** for real-time PC-to-FPGA testing; verified round-robin arbitration, upstream backpressure, and 5-way port contention; **1,731 LUTs / 3,656 FFs** (<3% of Artix-7 100T) at 0.127 W.
- **Runner-up** position at a national-level hardware hackathon in Mumbai, competing among **82 teams** across India.

Autonomous Ornithopter (Flapping-Wing UAV) Technology Demonstrator

Space Applications Centre (SAC) ISRO RESPOND BASKET 2024 (RES-SAC-2024-005) - Ongoing

- Building embedded flight avionics for an autonomous ornithopter UAV under Dr. Parth Thakar, HoD ECE, PDEU; project targets **autonomous powered flight** with **NAVIC-based positioning**, live video payload, and **IP65** ingress compliance.
- Working on closed-loop **PID attitude stabilization** across the full **6-DOF** flight envelope with **IMU-based sensor fusion** (accelerometers, gyros, inclinometers) for dynamic characterization including vibrations, drift, and landing shocks.
- Scoping onboard telemetry stack, fail-safe firmware, and autonomous navigation logic; planned validation via **HIL simulation** in **ROS2** middleware prior to physical prototype integration.

Space Invaders on FPGA

Real-Time Streaming Graphics System

- Implemented a real-time **VGA 640×480 @ 60Hz** Space Invaders arcade game in Verilog using **AXI-Stream** graphics pipeline tested on Nexys A7 (Artix-7 100T)
- Integrated a **PS5 DualSense controller** via an **ESP32 BLE** bridge; UART receiver (115200 baud, 16× oversampling) routes 8-byte packets to game logic.
- Designed modular subsystems: player ship, projectile system, 3×8 enemy grid with **AABB collision detection**, and a state machine (MENU → PLAYING → VICTORY/GAMEOVER).

Custom ROM Development

AOSP-Based OS Compilation

- Compiled and deployed **PixelExperience Android firmware** for *spes* (bootloader-unlocked smartphone) by modifying **device trees, BoardConfig.mk, kernel sources, and proprietary vendor blobs**.
- Configured build scripts, managed source dependencies, and optimised compilation with **ccache** and custom shell scripts; resolved integration issues with **hardware abstraction layers** (HALs) and vendor modules.

Leadership & Volunteering

IEEE Student Branch – PDEU

General Secretary & Treasurer — *Feb 2026 – Present*

- Overseeing **branch administration, finances, and planning**; coordinate across technical and non-technical verticals.

Technical Head — *Mar 2025 – Feb 2026*

- Led the branch in organizing **workshops and hackathons** on IoT, RF antennas, brain-computer interfaces, Git/GitHub, and Linux for **100+ participants**.

IEEE RAS Student Branch Chapter – PDEU — *Sep 2025 – Present*

Vice Chair

- Driving robotics and automation outreach initiatives; organising technical events and coordinating chapter activities since founding.

NEEV – IIT Gandhinagar — *May 2025 – Jun 2025*

Teaching Assistant

- Led sessions for **Basic Computer Skills and Spoken English training** for **rural youth and women**; simplified complex concepts to enhance digital literacy and communication confidence.

Editorial Team – SoT PDEU — *Feb 2025 – Present*

Content Editor

- Serving as Content Editor for the **annual department magazine *(Sancharini)*** and newsletters for the Department of ICT & ECE under Prof. Abhishek Kumar's guidance.

Education

Pandit Deendayal Energy University — Gandhinagar, Gujarat

B.Tech – Electronics and Communication Engineering — *Expected 2028*

- **Relevant Coursework:** C Programming, Python, Verilog HDL, Signals & Systems, Calculus, Linear Algebra, Analog Electronics, Digital Design, CAD

Certifications & Achievements

RTL to GDSII Workshop — *Apr 2026*

Department of ICT & ECE, School of Technology PDEU

- Completed full **ASIC tapeout flow** on **SAED 32nm RVT** PDK using **Synopsys DC, IC Compiler II, and PrimeTime**.
- *Task completed:* **equation ($Y = 4^X$, 2-bit unsigned)** with zero DRC/STA violations across both SS and FF corners. *Constraints:* **L-shaped floorplan** (side_length {8 8 4 4 8 8}) with pins on side 6; synthesis with **AND cells set as dont_use**, steering the netlist to NAND/NOR/INV primitives, **setup WNS 1.62 ns**, total cell area **50.32 μm^2**.

ROBOFEST 5.0 (Intelligent Ground Vehicle Competition Category, Finalist) — *Jan 2026*

Gujarat Council on Science and Technology (GUJCOST)

- **2nd position nationwide** during the Ideation Stage among teams across India. Successfully **cleared the Proof-of-Concept Stage**.

Winter School on Semiconductor Technology — *Dec 2025*

Centre for Nano Science and Engineering (CeNSE), IISc Bangalore

- Awarded **Certificate of Distinction**; covered semiconductor fabrication, nano-engineering processes, and industry applications.

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